What is claimed is:

1. A method of arbitrating a system bus that is shared by a CPU, which is a first master device, and second and third master devices, the method comprising:

storing a first bus occupancy rate for each of the CPU and the second and third master devices and a variable bus occupancy rate;

applying a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices to a bus arbiter, in response to an activation of an interrupt signal provided to the CPU;

applying a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first bus occupancy rates for the second and third master devices to the bus arbiter, in response to an inactivation of the interrupt signal; and

controlling a priority for use of the system bus in accordance with the second and third bus occupancy rates for the CPU and the first bus occupancy rates of the second and third master devices that are applied to the bus arbiter.

2. A method of arbitrating a system bus that is shared by a CPU, which is a first master device, and second and third master devices, the method comprising:

storing a first bus occupancy rate for each of the CPU and the second and third master devices and a variable bus occupancy rate;

applying a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices to a bus arbiter in response to an activation of a privilege mode signal generated by the CPU;

applying a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first bus occupancy rates for the second and third master devices to the bus arbiter, in response to an inactivation of the privilege mode signal; and

controlling a priority for use of the system bus in accordance with the second and third bus occupancy rates for the CPU and the first bus occupancy rates of the second and third master devices that are applied to the bus arbiter.

3. A method of arbitrating a system bus that is shared by a CPU, which is a first master device, and second and third master devices, the method comprising:

storing a first bus occupancy rate for each of the CPU and the second and third master devices and a variable bus occupancy rate;

applying a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices to a bus arbiter, in response to an activation of an interrupt signal provided to the CPU or a privilege mode signal generated by the CPU;

applying a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first bus occupancy rates for the second and third master devices to the bus arbiter, in response to an inactivation of the interrupt signal or the privilege mode signal; and

controlling a priority for use of the system bus in accordance with the second and third bus occupancy rates for the CPU and the first bus occupancy rates of the second and third master devices that are applied to the bus arbiter.

4. A system including a CPU, which is a first master device, and second and third master devices, which share a system bus, the system comprising:

a device storing first bus occupancy rates for the second and third master devices and a variable bus occupancy rate for increasing or decreasing a first bus occupancy rate for the CPU; and

a bus arbiter receiving either a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to an interrupt signal provided to the CPU, receiving the first bus occupancy rates for the

second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

5. The system of claim 4, wherein the bus arbiter comprises a multiplexer which receives either the second bus occupancy rate for the CPU or the third bus occupancy rate for the CPU in response to the interrupt signal provided to the CPU.

6. A system including a CPU, which is a first master device, and second and third master devices, which share a system bus, the system comprising:

a device storing first bus occupancy rates for the second and third master devices and a variable bus occupancy rate for increasing or decreasing a first bus occupancy rate for the CPU; and

a bus arbiter receiving either a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to a privilege mode signal generated by the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

7. The system of claim 6, wherein the bus arbiter comprises a mutiplexer which receives either the second bus occupancy rate for the CPU or the third bus occupancy rate for the CPU in response to the privilege mode signal generated by the CPU.

8. A system including a CPU, which is a first master device, and second and third master devices, which share a system bus, the system comprising:

a device storing first bus occupancy rates for the second and third master devices and a variable bus occupancy rate for increasing or decreasing a first bus occupancy rate for the CPU; and

a bus arbiter receiving either a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to an interrupt signal provided to the CPU or a privilege mode signal generated by the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

9. The system of claim 8, wherein the bus arbiter comprises an OR gate for receiving the interrupt signal and the privilege mode signal.

10. The system of claim 8, wherein the bus arbiter comprises a multiplexer which receives either the second bus occupancy rate for the CPU or the third bus occupancy rate for the CPU in response to the interrupt signal or the privilege mode signal.

11. A multi-layer bus system in which a CPU, which is a first master device, and second and third master devices use their dedicated buses, the multi-layer bus system comprising:

first, second, and third system buses exclusively used by the CPU and the second and third master devices, respectively; and

a slave device coupled to each of the first through third system buses,

wherein the slave device comprises:

a device storing first bus occupancy rates for the second and third master devices and a variable bus occupancy rate for increasing or decreasing a first bus occupancy rate for the CPU; and

a bus arbiter receiving either a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to an interrupt signal provided to the CPU or a privilege mode signal generated by the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

12. The multi-layer bus system of claim 11, wherein the bus arbiter comprises an OR gate for receiving the interrupt signal and the privilege mode signal.

13. The multi-layer bus system of claim 11, wherein the bus arbiter comprises a multiplexer which receives either a second bus occupancy rate for the CPU or the third bus occupancy rate for the CPU in response to the interrupt signal or the privilege mode signal.

14. A PCI bus system comprising:

a PCI bus coupled to a plurality of slots;

a host device coupled to the PCI bus, the host device controlling the PCI bus system;

a device storing bus occupancy rates for a plurality of cards inserted into respective slots and a variable bus occupancy rate for increasing or decreasing the bus occupancy rates; and

a bus arbiter controlling a priority for use of the PCI bus in accordance with the bus occupancy rates for the cards in response to interrupt signals generated by the cards.

15. The PCI bus system of claim 14, wherein the host device is a PCI bridge circuit.

16. The PCI bus system of claim 14, wherein each card is one of a graphic card, a network card, and a sound card.

17. A card bus system comprising:

a plurality of cards coupled to a card bus;

a host device coupled to the card bus, controlling the card bus system;

a device storing bus occupancy rates for the cards and a variable bus occupancy rate for increasing or decreasing the bus occupancy rates; and

a bus arbiter controlling a priority for use of the card bus in accordance with the bus occupancy rates for the cards in response to interrupt signals generated by the cards.